

FIG. 1
(PRIOR ART)

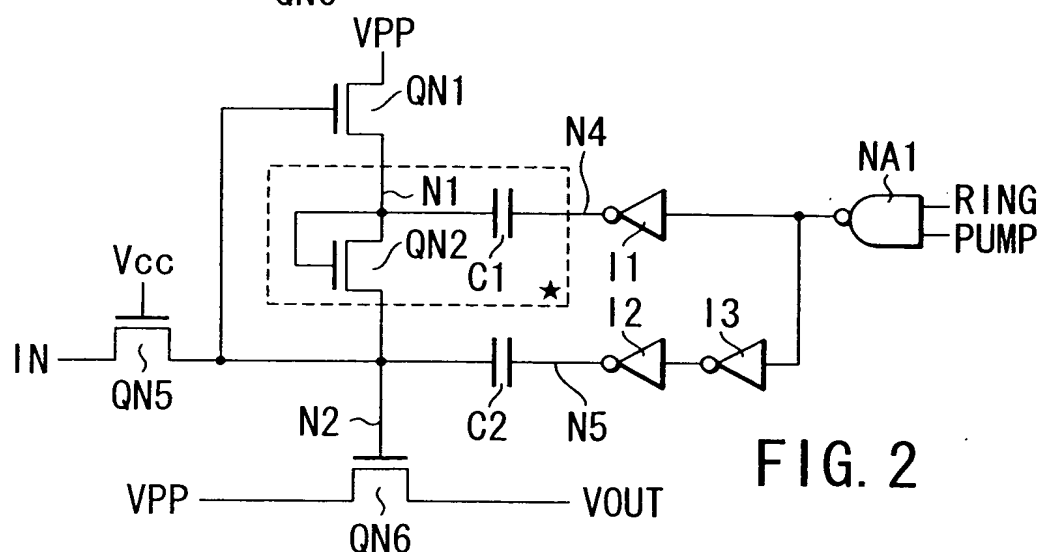


FIG. 2

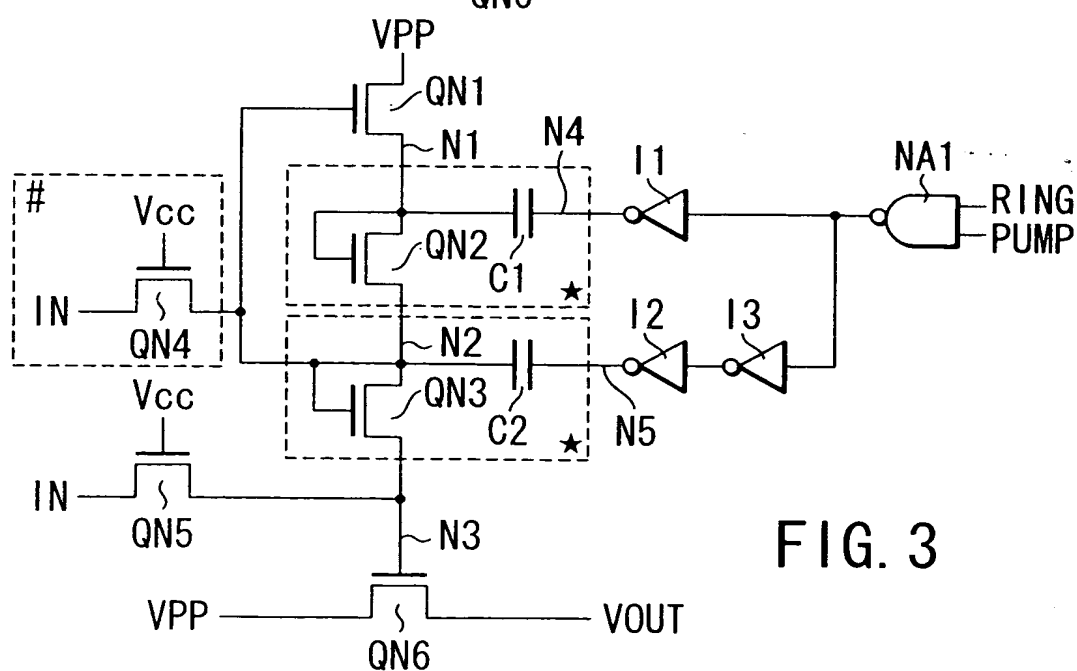
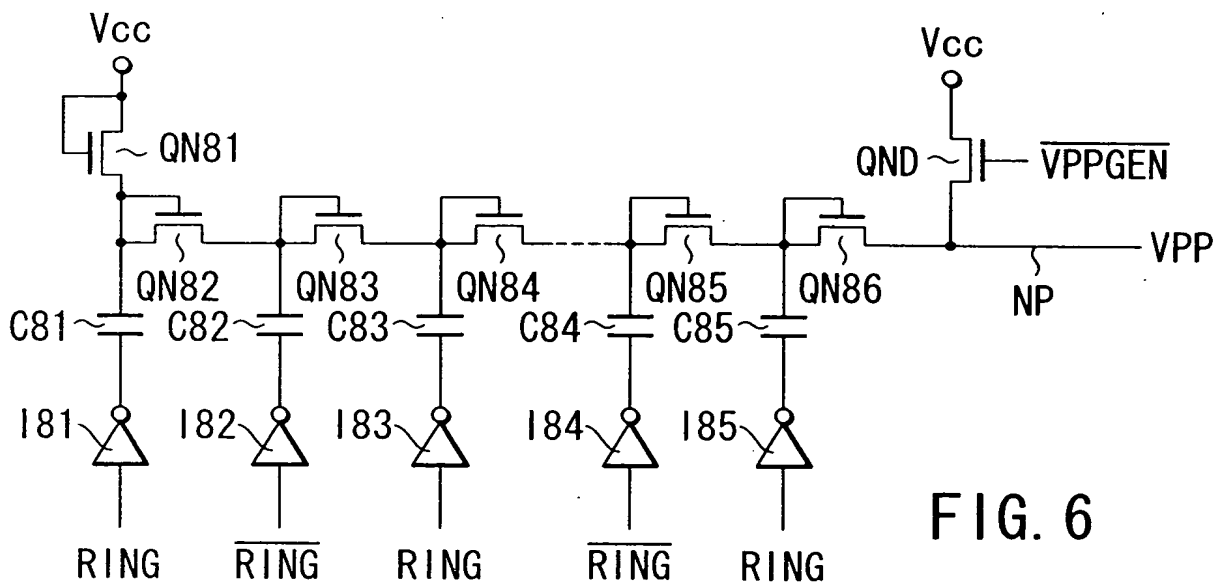
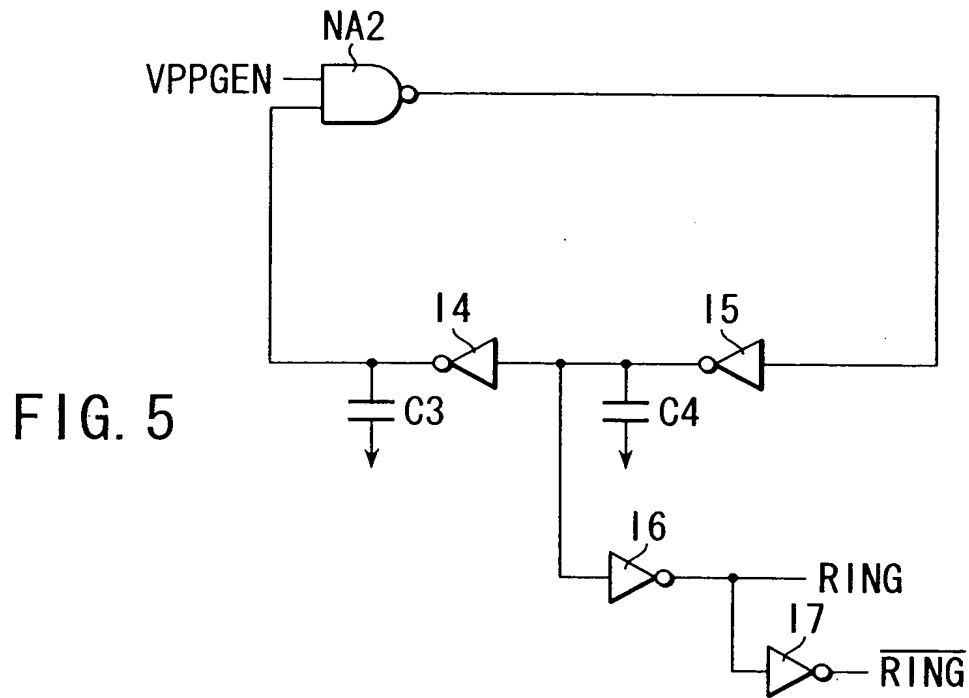
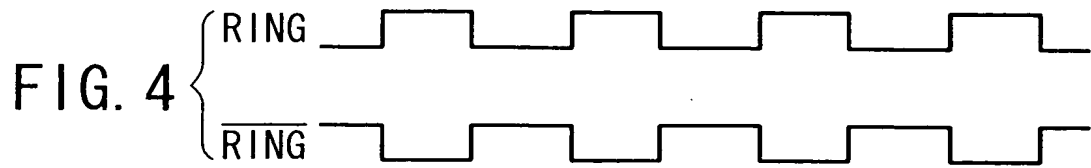


FIG. 3



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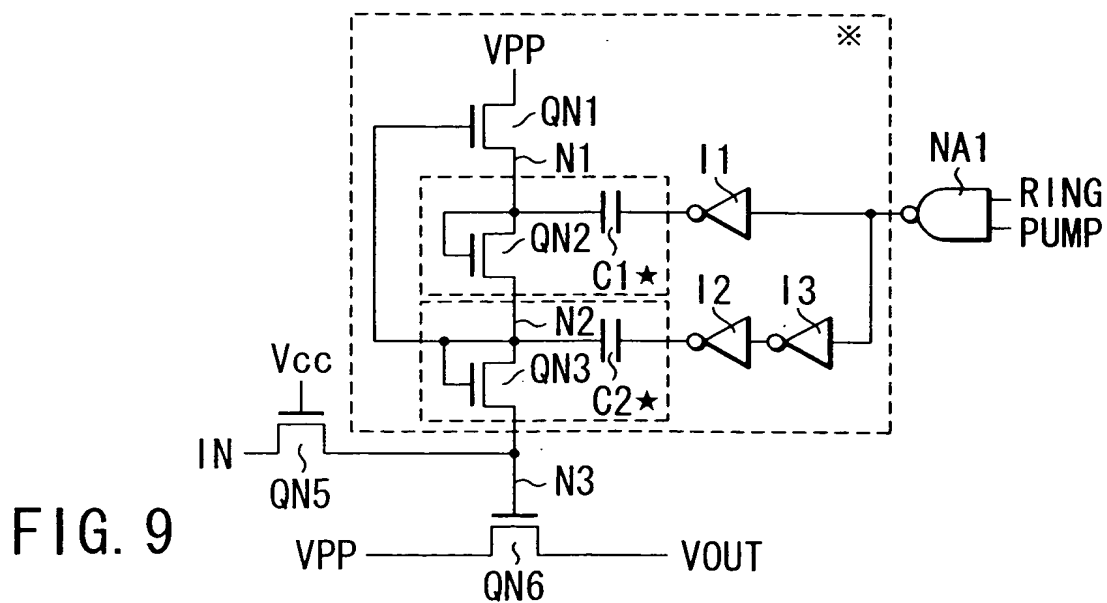
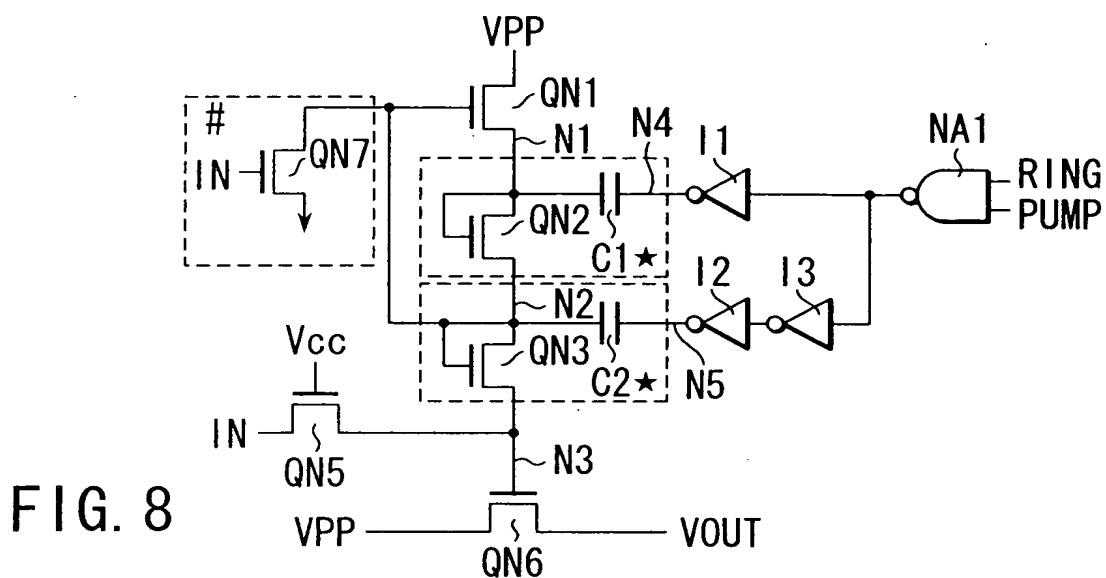
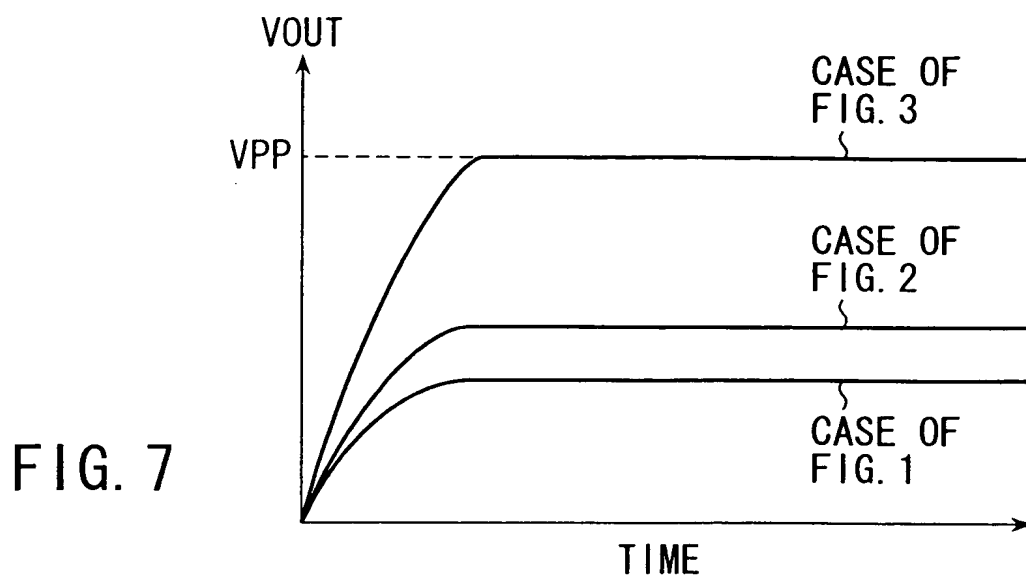


FIG. 10

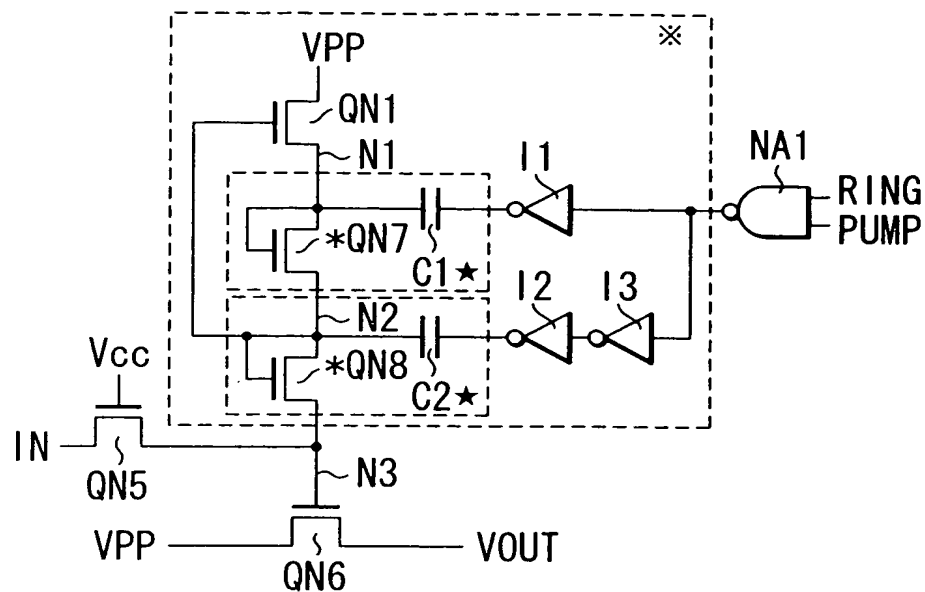


FIG. 11

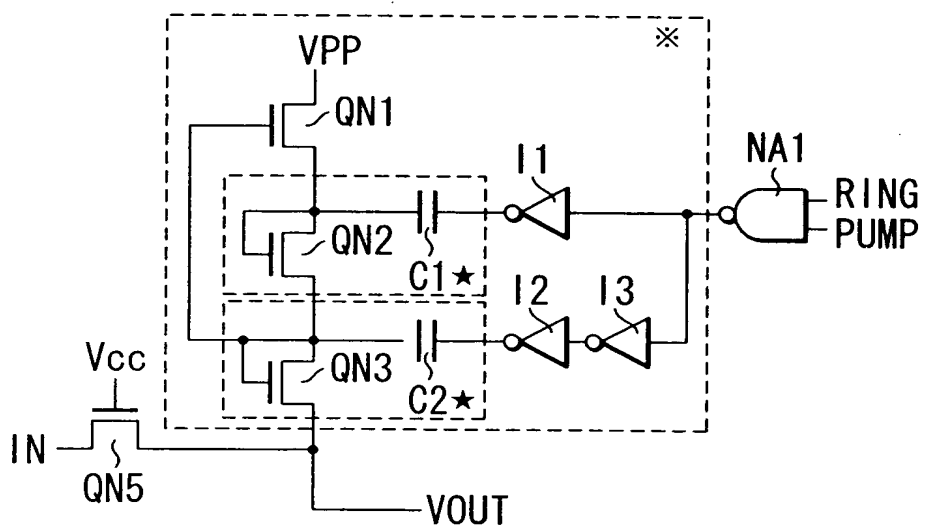


FIG. 12

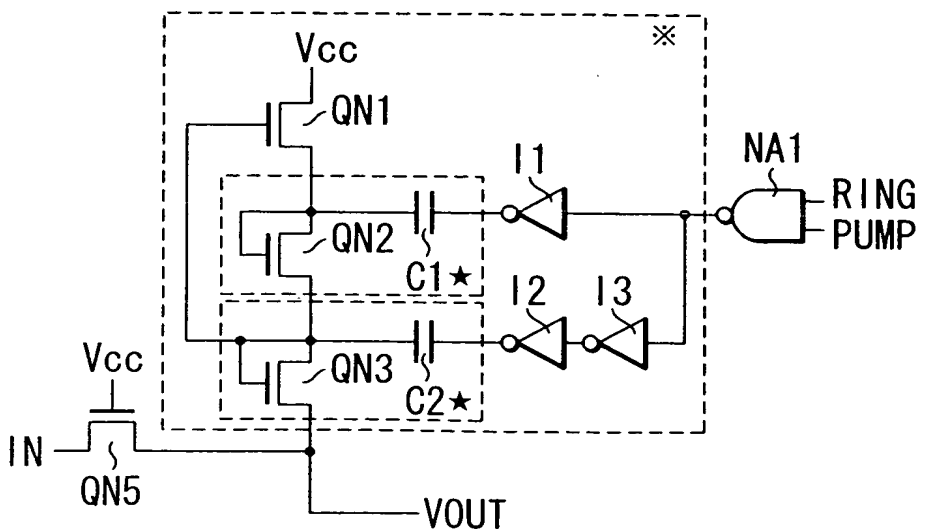


FIG. 13

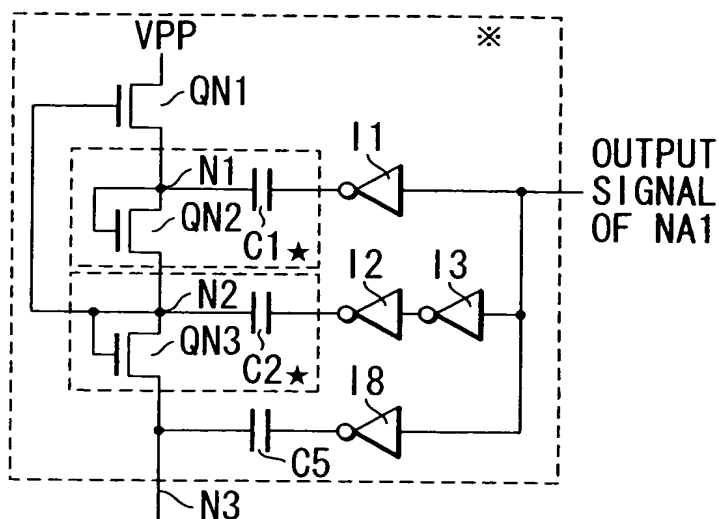


FIG. 14

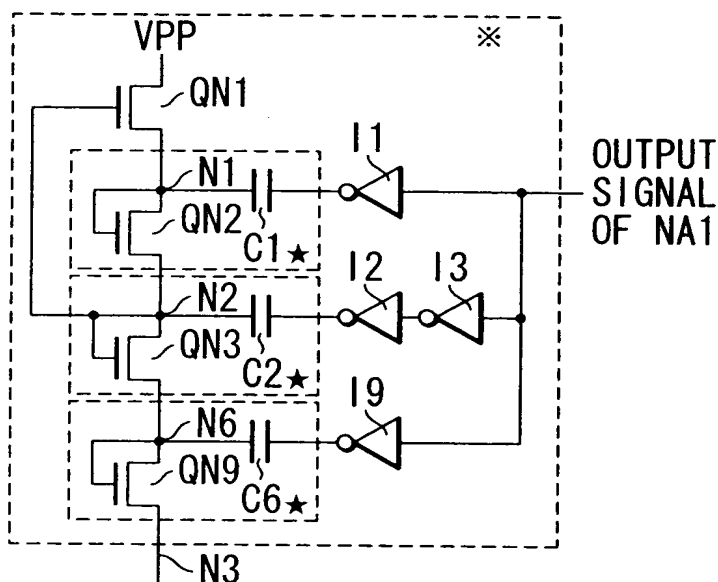


FIG. 15

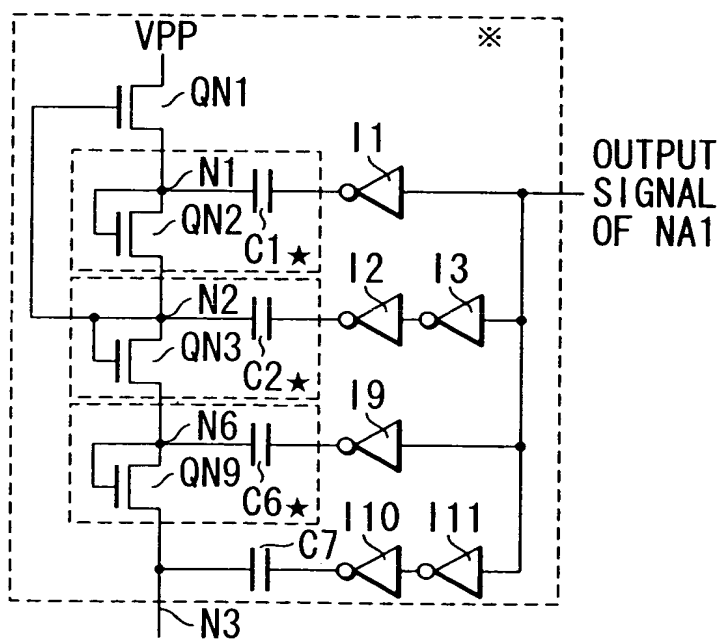


FIG. 16

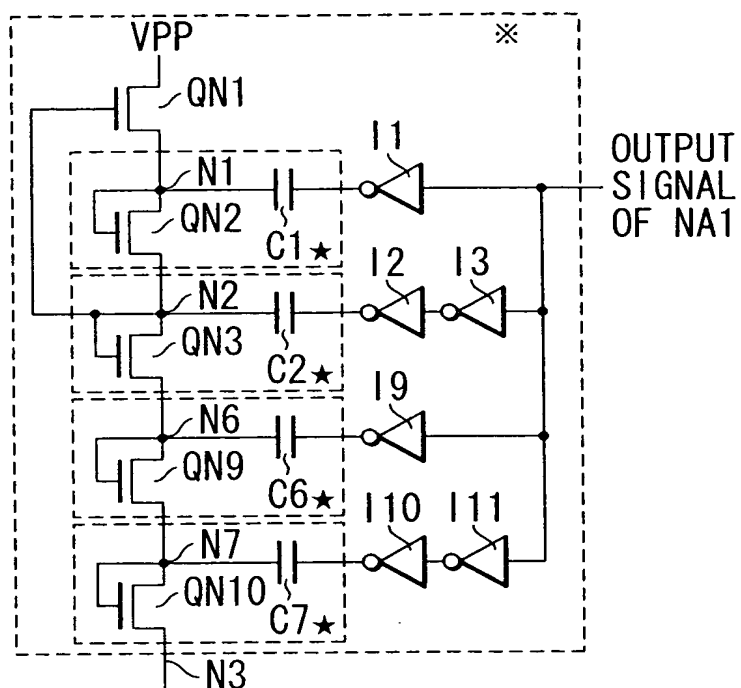
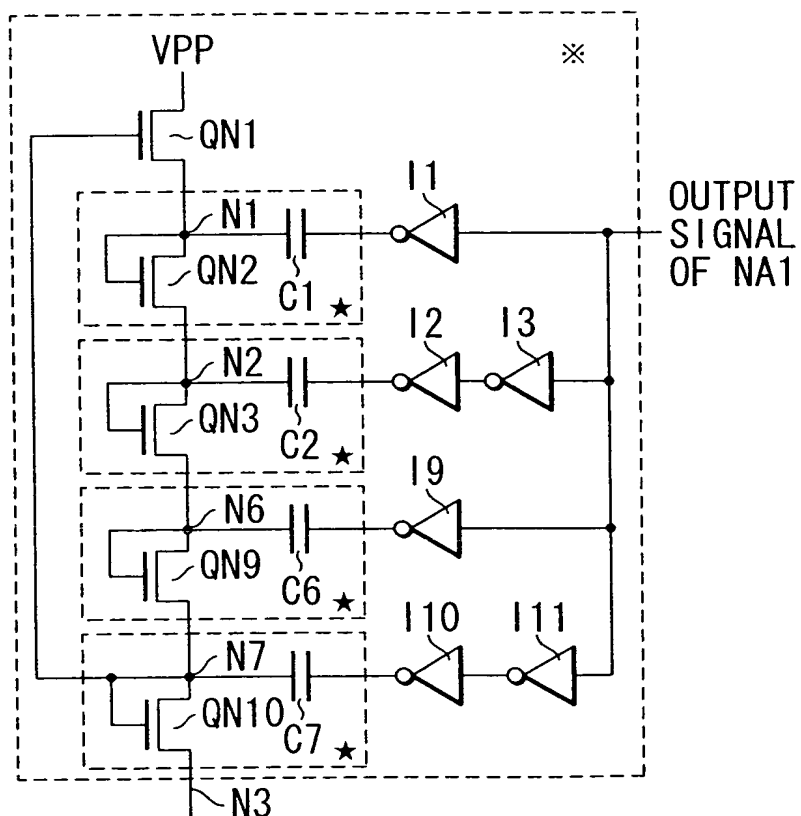


FIG. 17



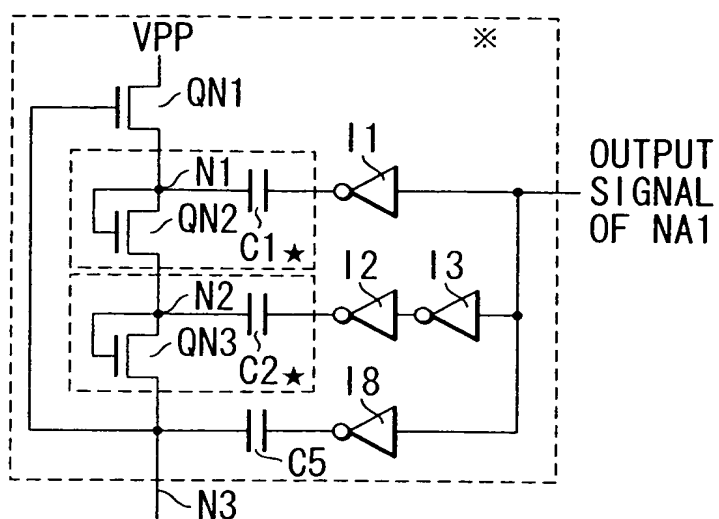


FIG. 19

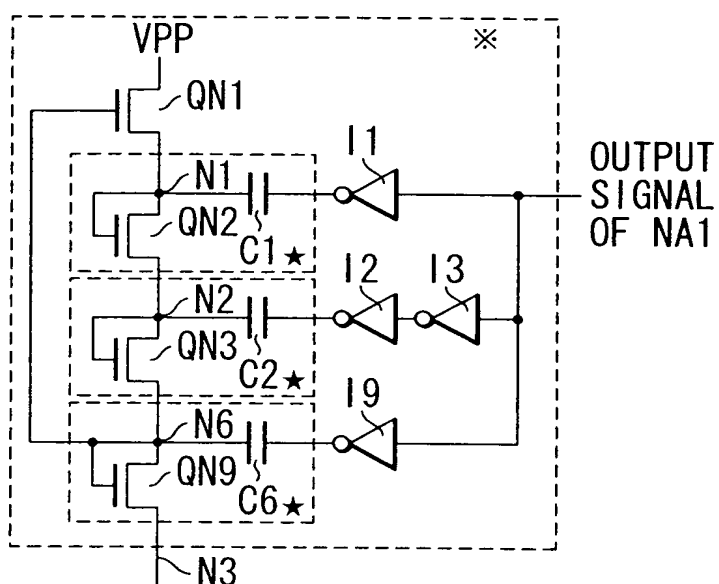


FIG. 20

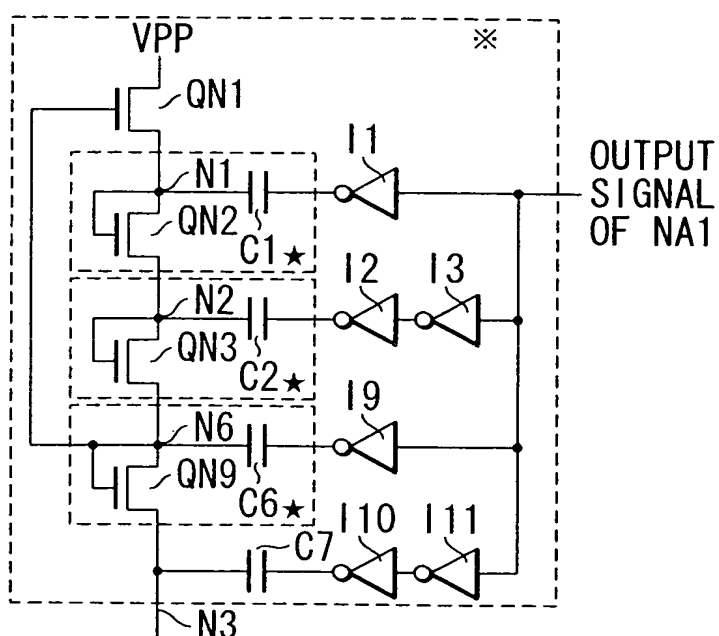


FIG. 21

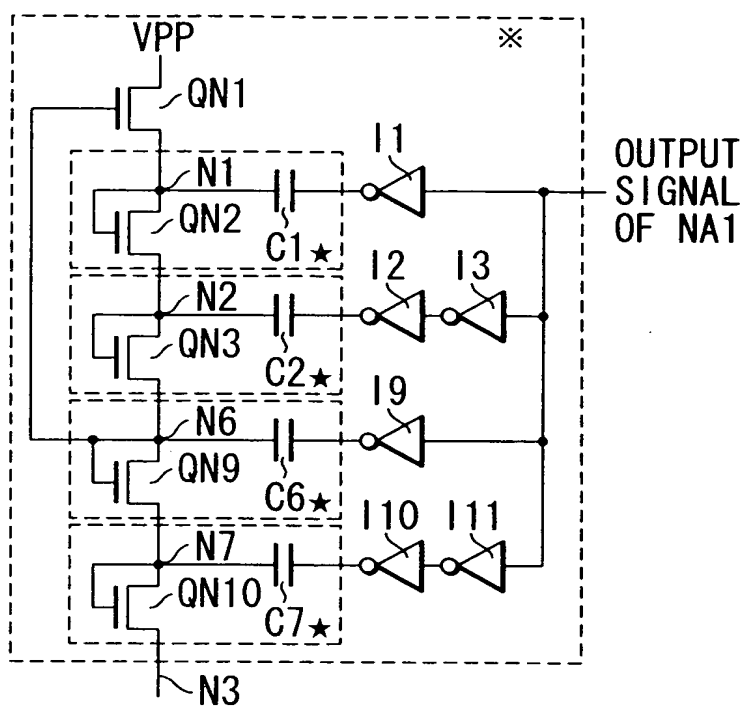
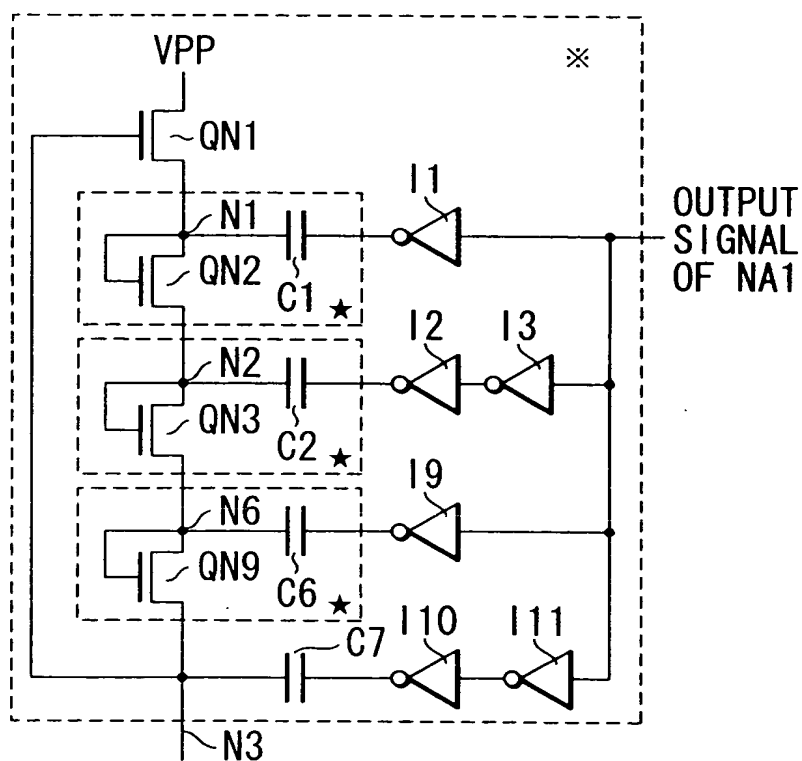


FIG. 22



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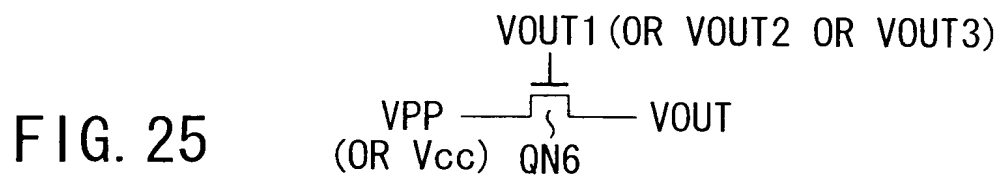
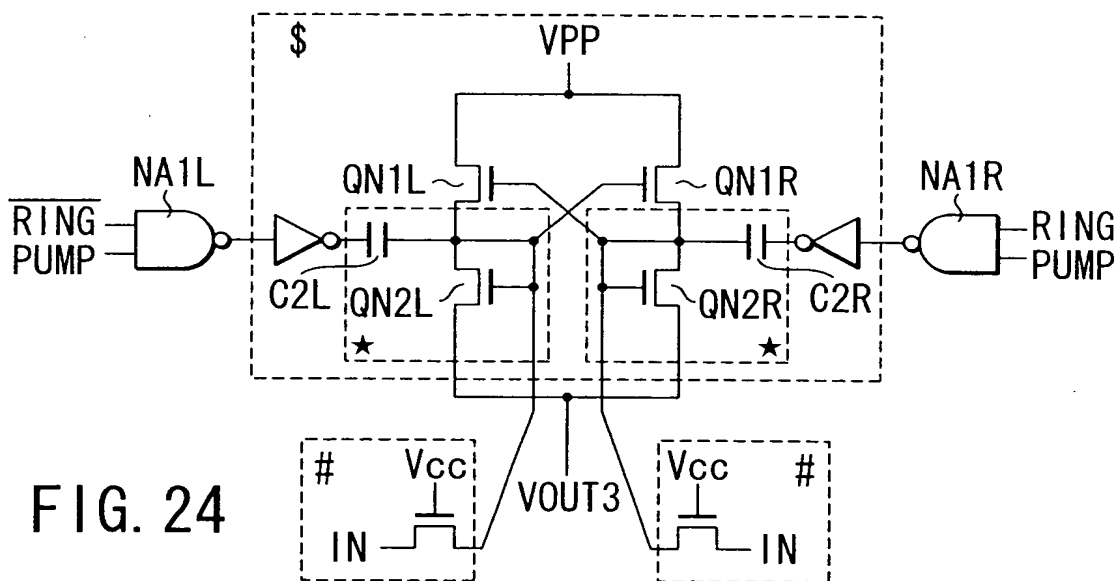
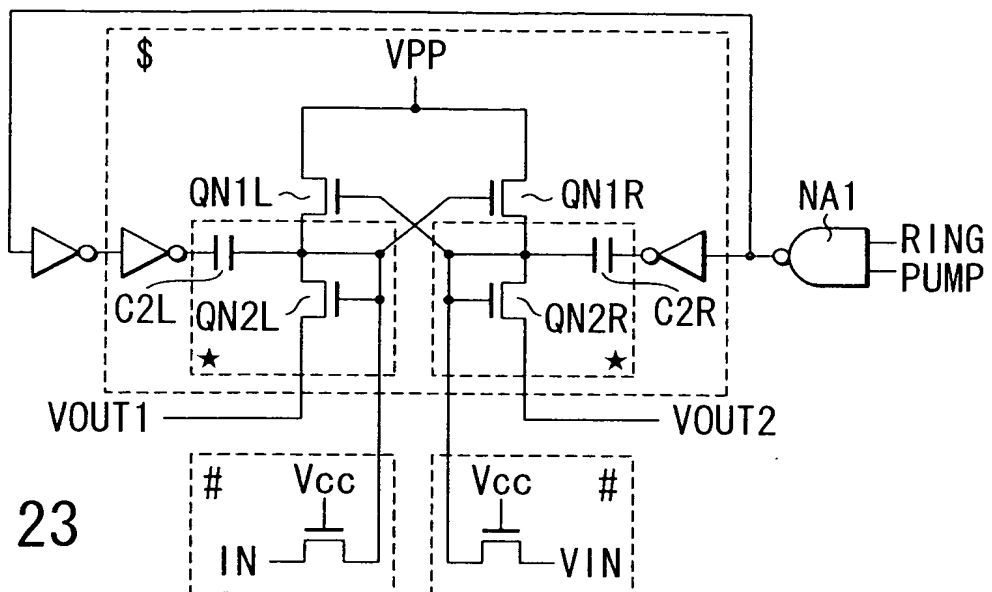


FIG. 29

FIG. 30

FIG. 31

FIG. 32

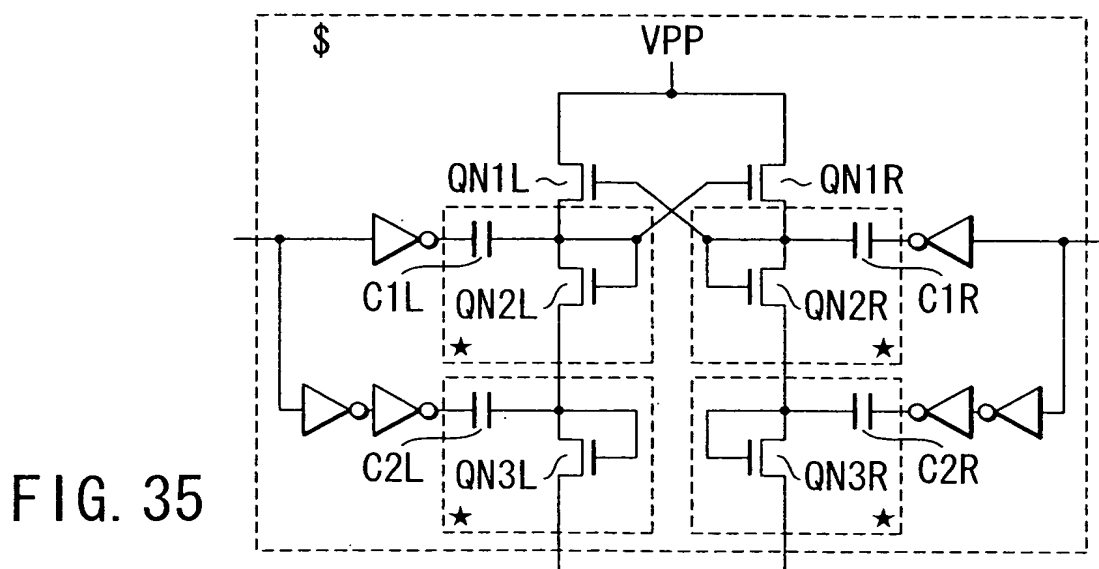
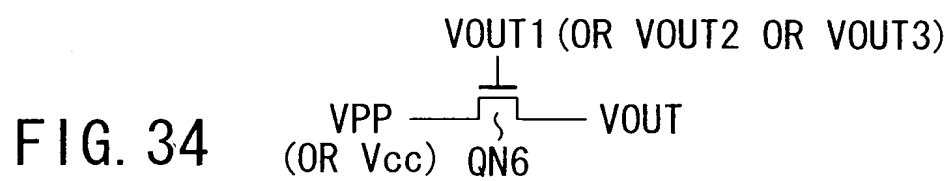
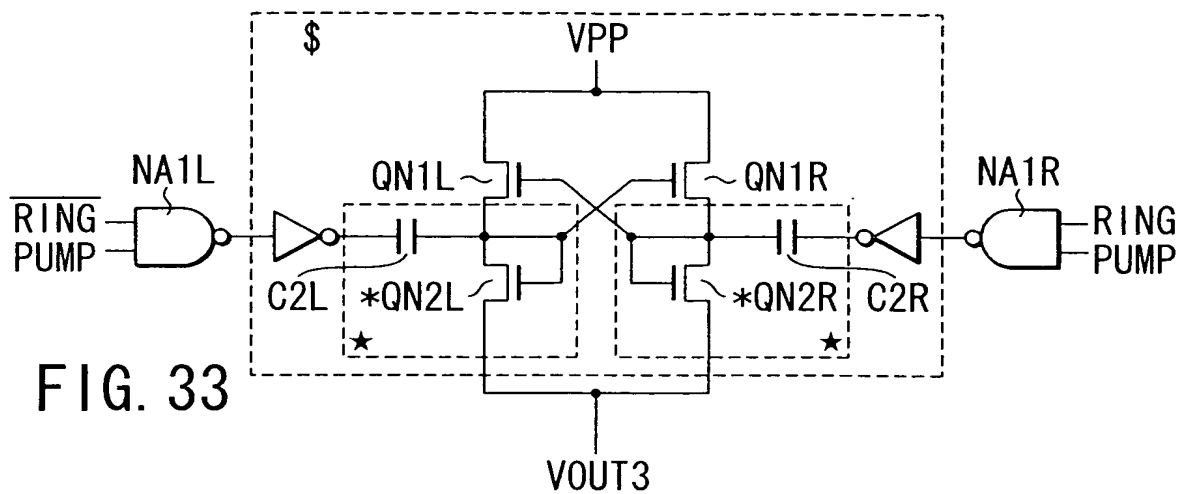


FIG. 36

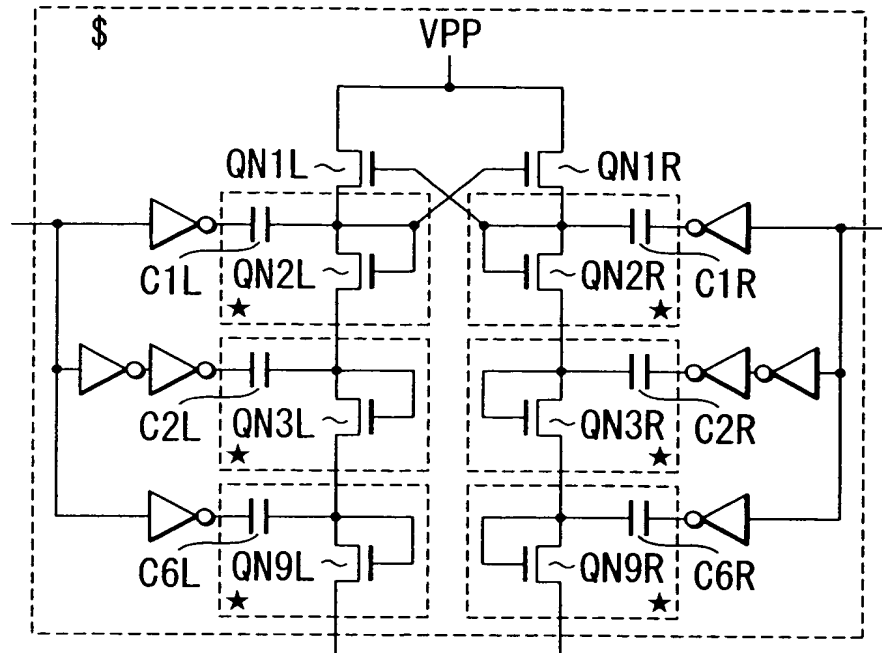


FIG. 37

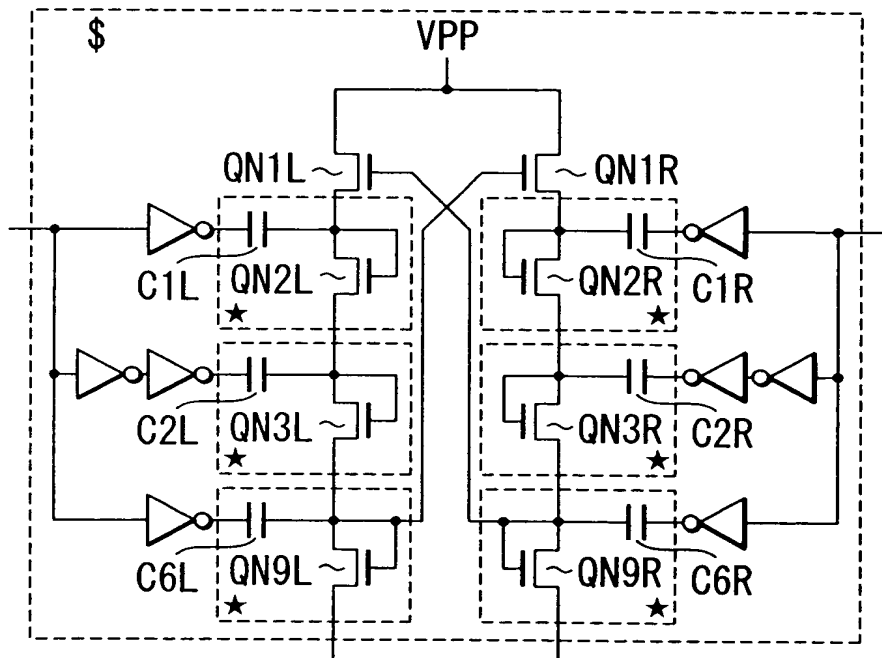
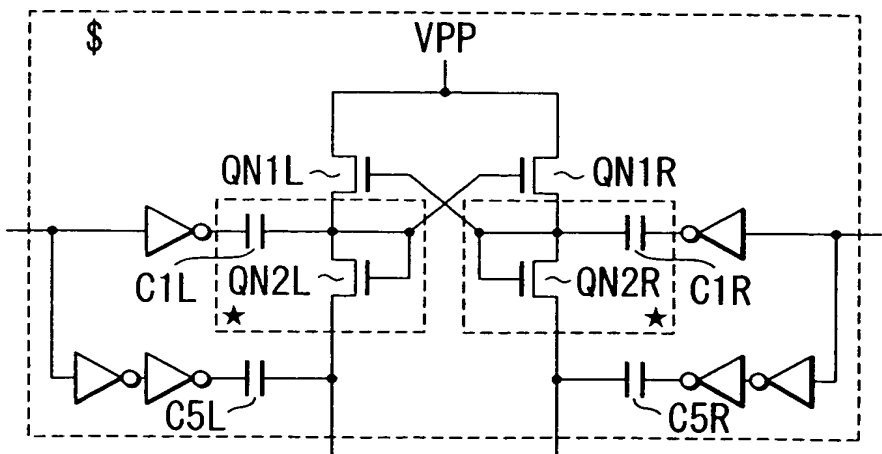


FIG. 38



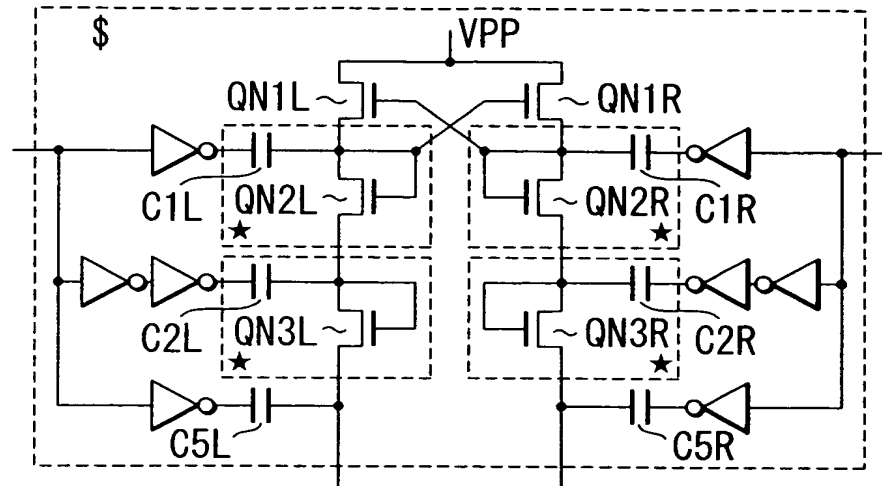


FIG. 39

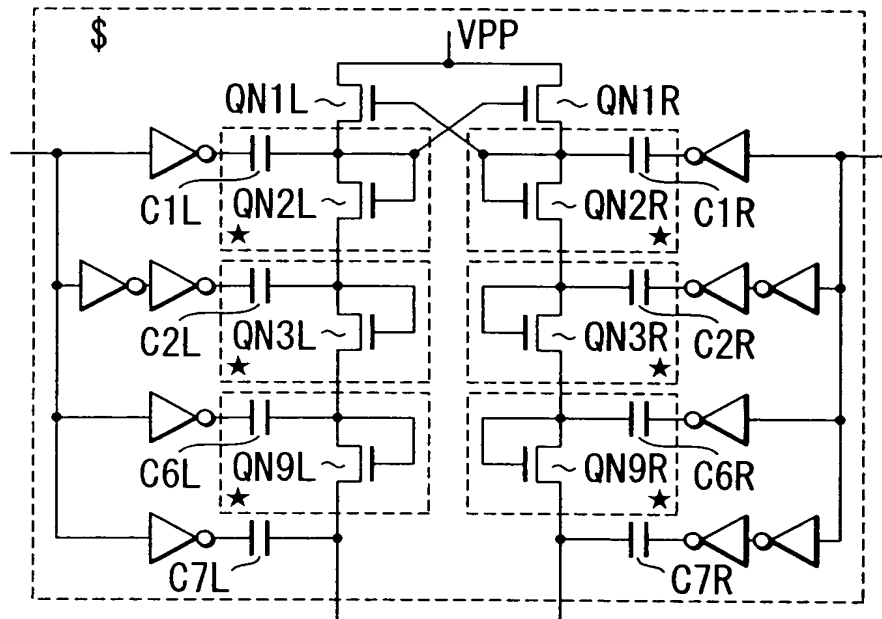


FIG. 40

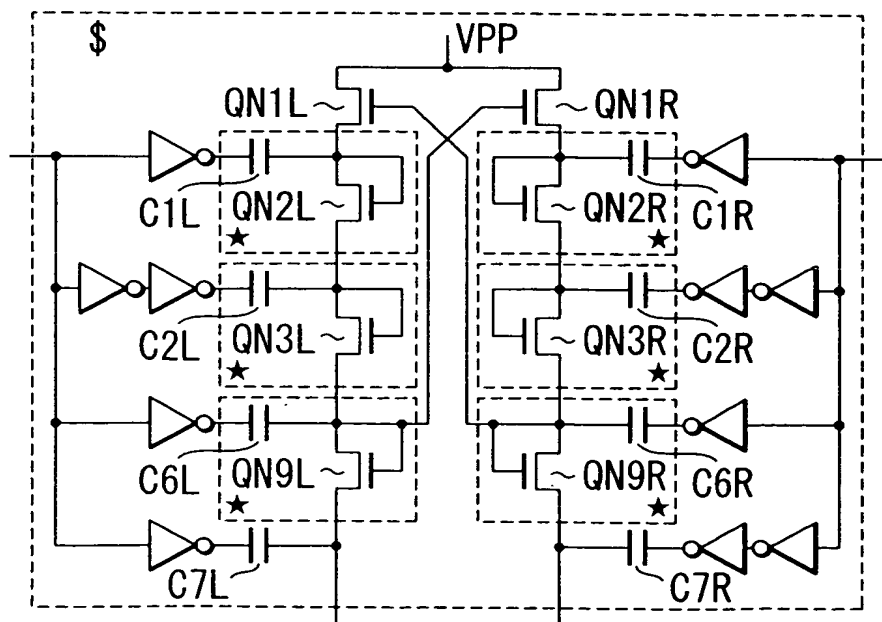


FIG. 41

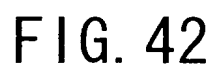




FIG. 48

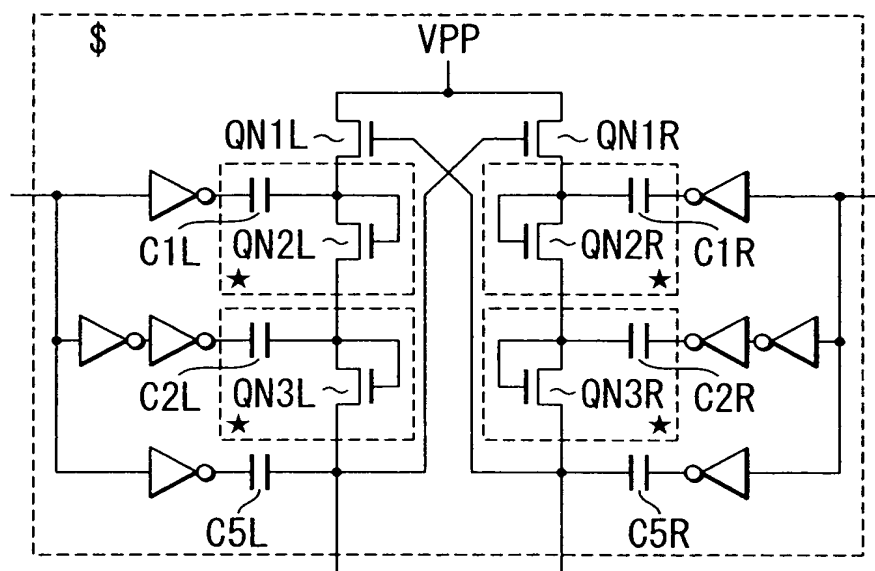


FIG. 49

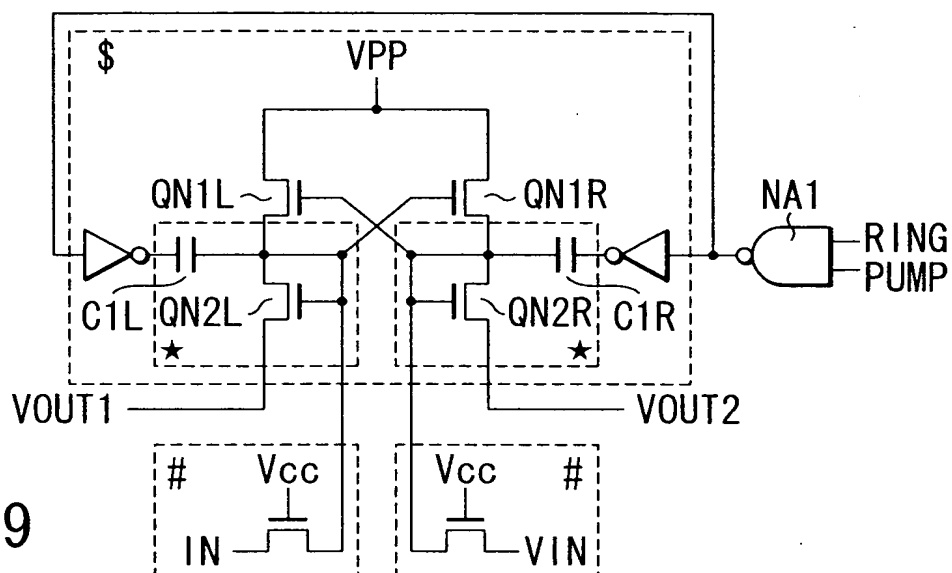
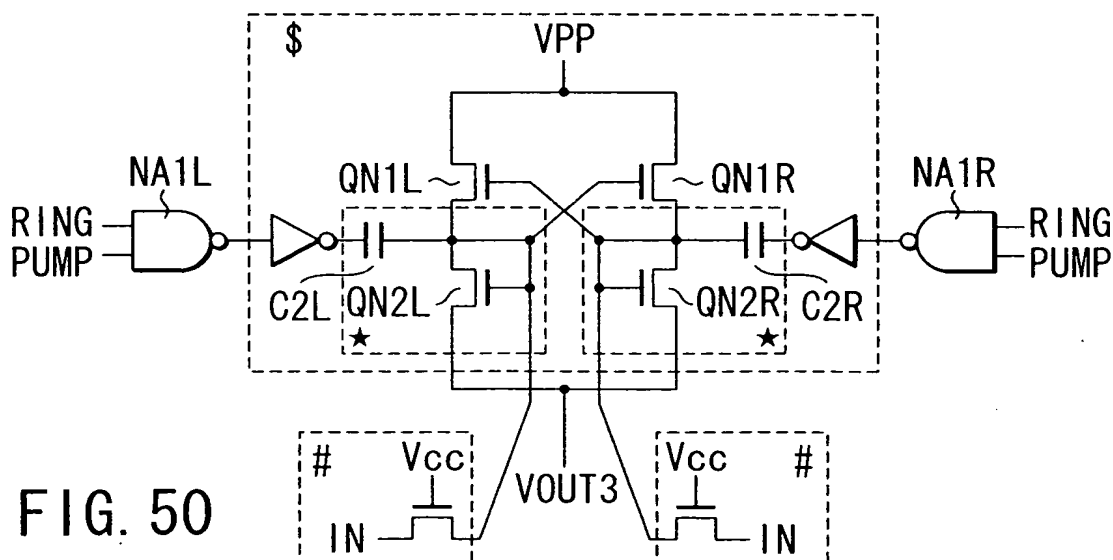


FIG. 50



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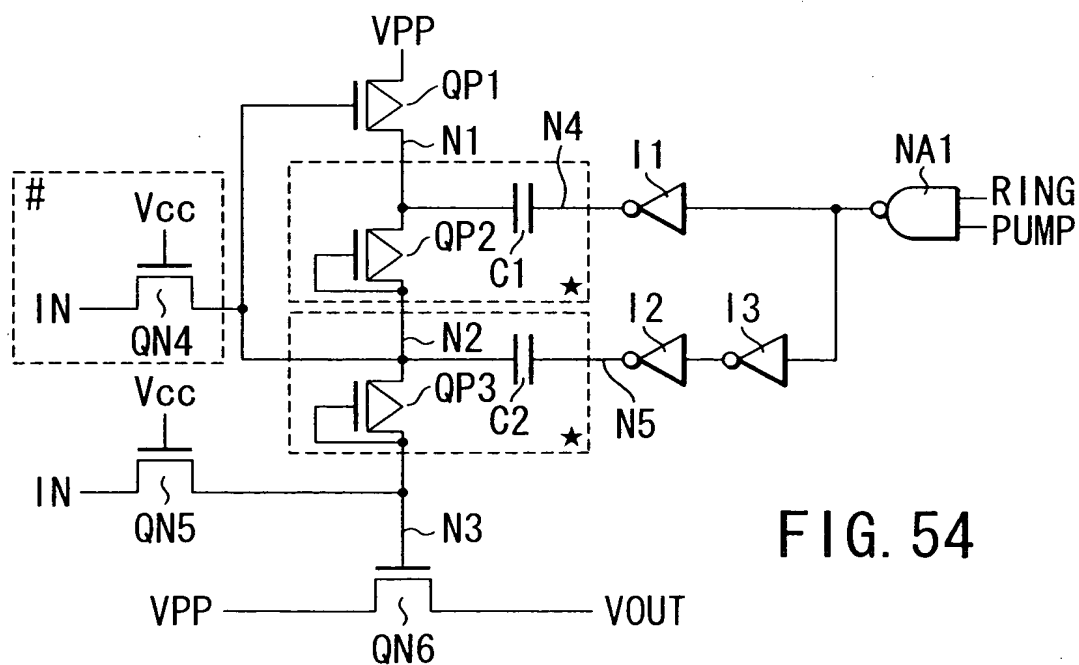
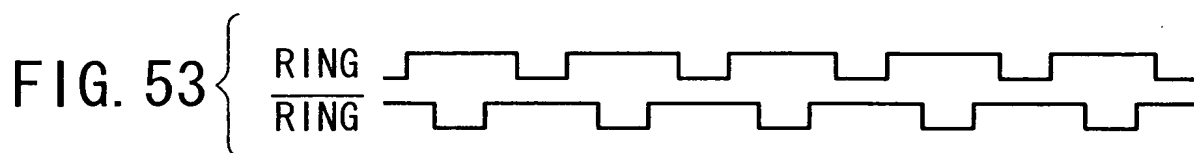
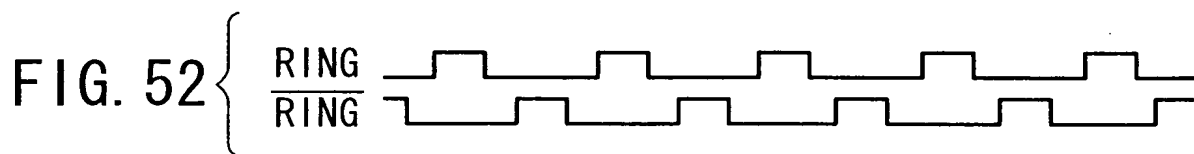
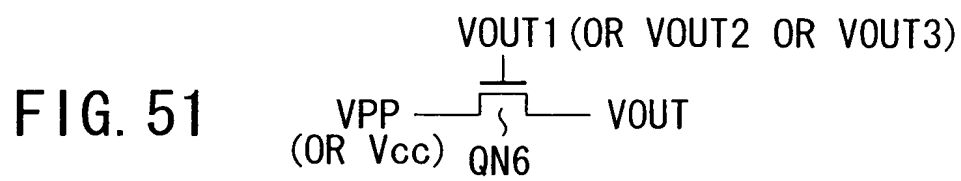


FIG. 54

The circuit diagram, labeled FIG. 56, shows a differential amplifier with a ring pump output stage. The input stage consists of a differential pair of PMOS transistors QP4 and QP5, and a common source NMOS transistor QP6. The gates of QP4 and QP5 are connected to an input signal IN. The gates of QP4, QP5, and QP6 are connected to a bias network consisting of a PMOS transistor QP1 and two NMOS transistors N1, N2, and N3. The gates of N1 and N2 are connected to -VEE, and the gates of N3 and QP6 are connected to -VEE. The drains of QP4 and QP5 are connected to a load network consisting of a PMOS transistor QP2 and two NMOS transistors N4, N5, and N6. The gates of N4 and N5 are connected to -VEE, and the gates of N6 and QP2 are connected to -VEE. The drains of QP2 and QP6 are connected to -VEE. The outputs of the differential pair are connected to a ring pump circuit consisting of three inverters I1, I2, and I3, and a NAND gate NA1. The output of the ring pump is labeled RING PUMP.

FIG. 56